We claim:

1. A programmable processor comprising:

an instruction path;

a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

a register file operable to receive and store data from the data path and communicate the stored data to the data path; and

an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path,

at least some of the instructions including a group floating-point instruction operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands;

at least some group floating-point instruction being a group floating-point multiply-and-add instruction, further operating on a third register partitioned into a plurality of floating-point operands,

the execution unit operable to multiply the plurality of floating-point operands in the first and second registers and add the plurality of floating-point operands in the third register, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a

catenated result having a plurality of partitioned fields for receiving the plurality of floating point values.

2. The processor of claim 1,

at least some group floating-point instruction being at least one member of the collection consisting of group floating-point subtract, group floating-point add, and group floating-point multiply,

operable to perform a subtract, add and multiply respectively on the plurality of floating-point operands in the first and second registers, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values; and

at least some group floating-point instruction being at least one member of the collection consisting of group floating-point set less, and group floating-point set greater or equal,

operable to perform a set-less and set-greater-or-equal operation, respectively, on the plurality of floating-point operands in the first and second registers, each producing a value to provide a plurality of values, each of the values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of values, wherein the value is zero if the operation produces a false result, and wherein the value is an identity value if the operation produces a true result; and

at least some of the instructions comprising performing data manipulations on multiple operands stored in partitioned fields of registers wherein the data manipulations comprise copying or rearranging operands.

3. The processor of claim 2 wherein the zero value and the identity value are values that construct a bit mask operable to select between alternate expressions using a bitwise Boolean operation.

4. The processor of claim 1 wherein the catenated result has a width of 128 bits.

5. The processor of claim 1 wherein the catenated result is provided to a register.

6. The processor of claim 1 wherein the defined precision is 16 bits.

7. The processor of claim 1 wherein the defined precision is a format comprising one sign bit, five exponent bits and ten significand bits.

8. The processor of claim 1 wherein the defined precision is 32 bits.

9. The processor of claim 1 wherein the precision of the group floating-point instructions is a format comprising one sign bit, eight exponent bits and 23 significand bits.

10. The processor of claim 1, wherein the defined precision is 64 bits.

11. The processor of claim 1, wherein the precision of the group floating-point instructions is a format comprising one sign bit, eleven exponent bits and 52 significand bits.

12. A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising:

a virtual memory addressing unit;

an instruction path and a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and

at least some of the instructions including a group floating-point instruction operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands;

at least some group floating-point instruction being a group floating-point multiply-and-add instruction, further operating on a third register partitioned into a plurality of floating-point operands,

the execution unit operable to multiply the plurality of floating-point operands in the first and second registers and add the plurality of floating-point operands in the third register,

each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values.

13. The system of claim 12,

at least some group floating-point instruction being at least one member of the collection consisting of group floating-point subtract, group floating-point add, and group floating-point multiply,

operable to perform a subtract, add and multiply respectively on the plurality of floating-point operands in the first and second registers, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values; and

at least some group floating-point instruction being at least one member of the collection consisting of group floating-point set less, and group floating-point set greater or equal,

operable to perform a set-less and set-greater-or-equal operation, respectively, on the plurality of floating-point operands in the first and second registers, each producing a value to provide a plurality of values, each of the values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of values, wherein the value is zero if the operation produces a false result, and wherein the value is an identity value if the operation produces a true result; and

at least some of the instructions comprising performing data manipulations on multiple

operands stored in partitioned fields of registers wherein the data manipulations comprise copying or rearranging operands.

14. The system of claim 13 wherein the zero value and the identity value are values that construct a bit mask operable to select between alternate expressions using a bitwise Boolean operation.

15. The system of claim 12 wherein the catenated result has a width of 128 bits.

16. The system of claim 12 wherein the catenated result is provided to a register.

17. The system of claim 12 wherein the defined precision is 16 bits.

18. The system of claim 12 wherein the defined precision is a format comprising one sign bit, five exponent bits and ten significand bits.

19. The system of claim 12 wherein the defined precision is 32 bits.

20. The system of claim 12 wherein the precision of the group floating-point instructions is a format comprising one sign bit, eight exponent bits and 23 significand bits.

21. The system of claim 12, wherein the defined precision is 64 bits.

22. The system of claim 12, wherein the precision of the group floating-point instructions is a format comprising one sign bit, eleven exponent bits and 52 significand bits.

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